Disk Drive Architecture Exploration

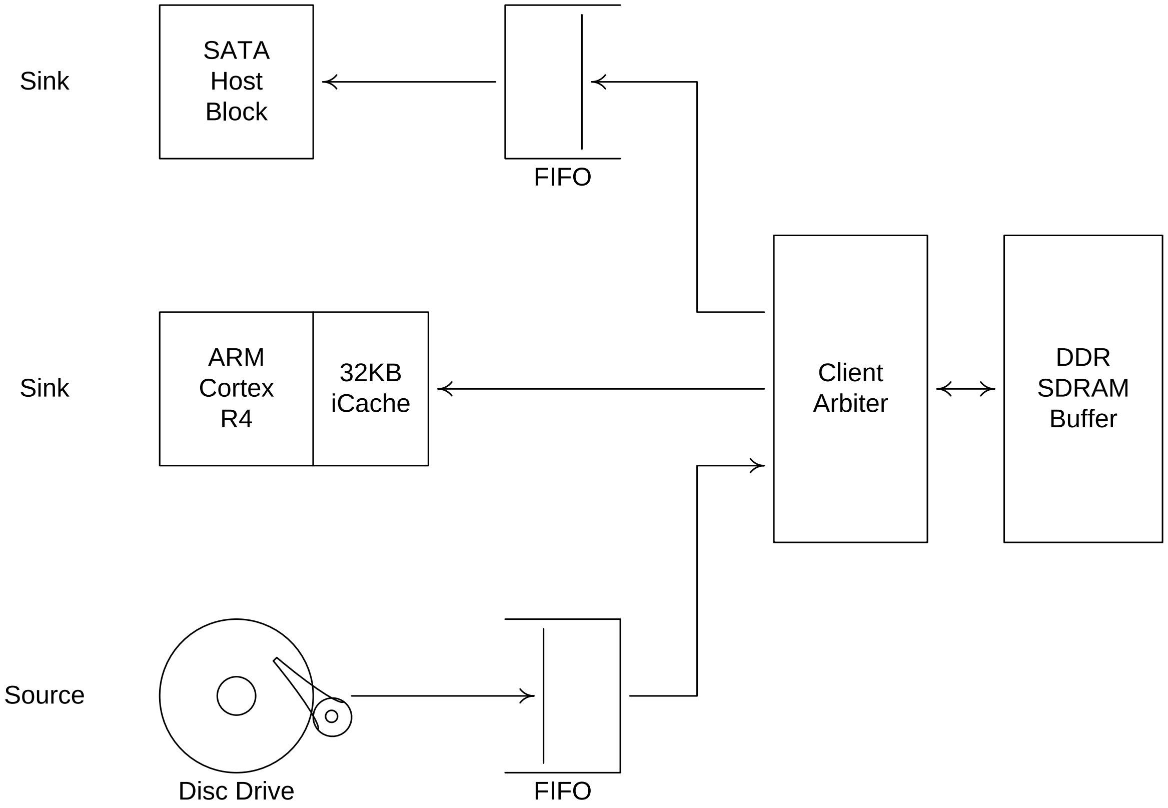
VisualSim

Mirabilis Design

Purpose Statement

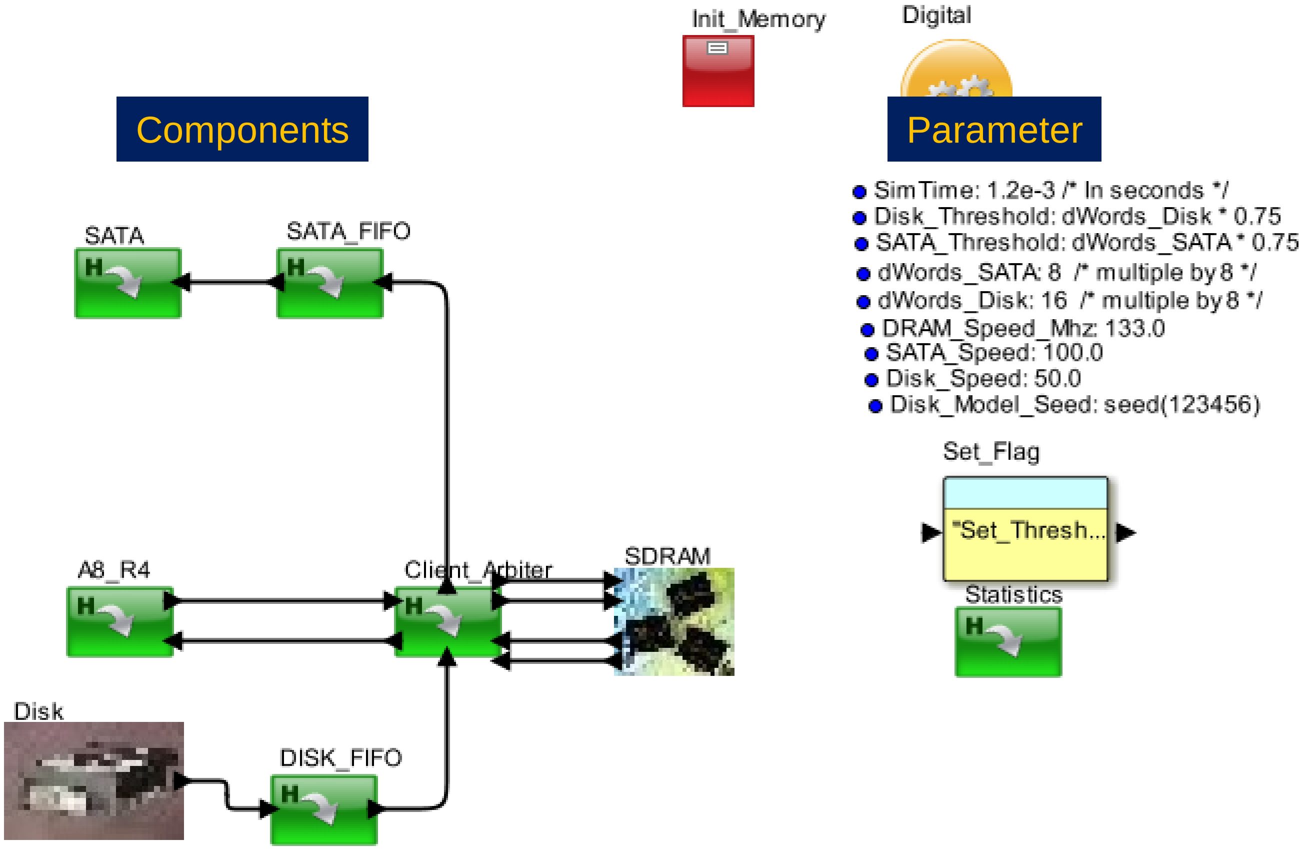
- System Level development environment to aid in design “what-if” scenario evaluation
- Tool should reside at the highest abstraction layers, but allow flow down to ESL modeling already underway.

Design Block Diagram



Simple Disc Read Buffer Simulation (3 Clients)

VisualSim Model- Top-Level

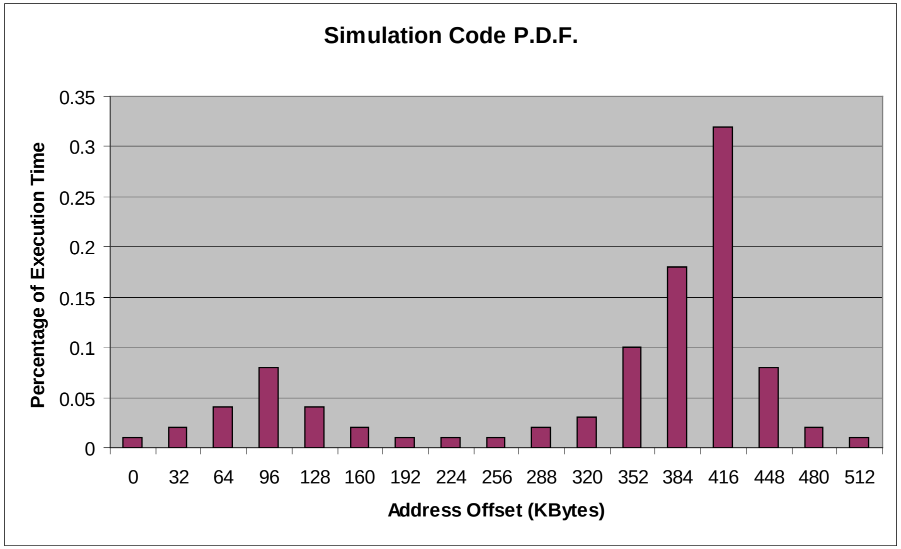


- SimTime: 1.2e-3 /* In seconds */
- Disk_Threshold: dWords_Disk * 0.75
- SATA_Threshold: dWords_SATA * 0.75
- dWords_SATA: 8 /* multiple by 8 */
- dWords_Disk: 16 /* multiple by 8 */
- DRAM_Speed_Mhz: 133.0
- SATA_Speed: 100.0
- Disk_Speed: 50.0
- Disk_Model_Seed: seed(123456)

SATA Host Block Characteristics

- Assume simple data transfer mode only, no command overhead, only data frames
  - Each Frame consists of 8 Bytes of Header, followed by the 8K data packet, followed by 8 Bytes of Trailer.
- Programmable transfer rates of 1.5/3.0/6.0 Gbps (150/300/600 Mbytes/s resulting from 8b/10b conversion)
- 8KByte Frame Size though temporary suspension of data allowed through SATA HOLD/HOLDA mechanism
  - Need to monitor how often HOLD is needed.
- Assume Frame transmission begins after FIFO almost Full signal or no sooner than 1us after last Frame.

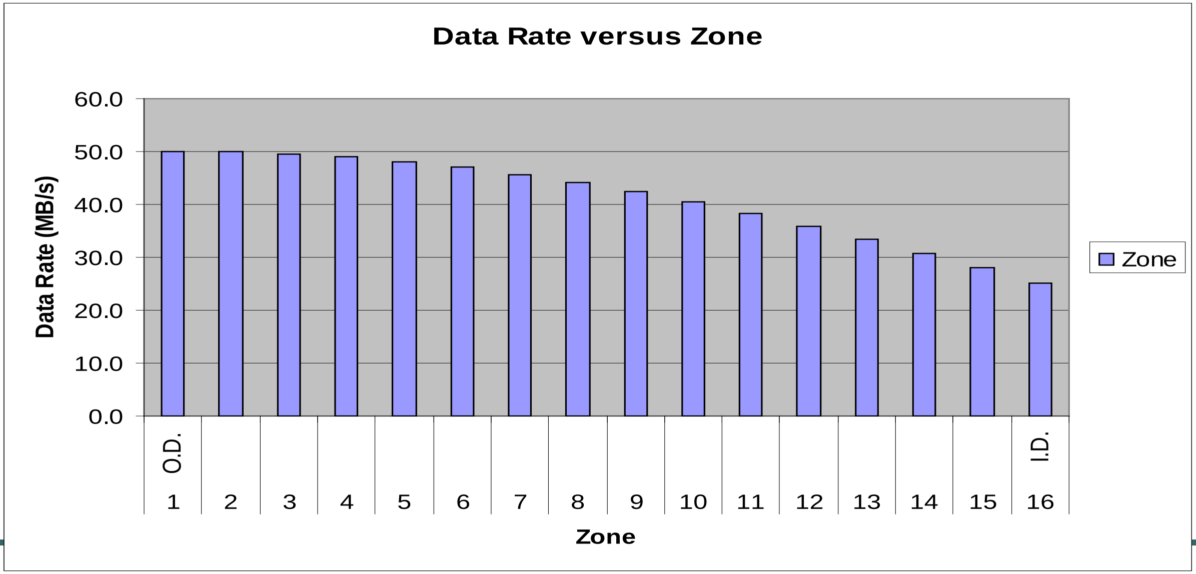
ARM Cortex R4 Characteristics



- Assume instruction pull only, all instructions reside within the SDRAM Buffer
  - Data accesses are strictly to ITCM (and unspecified)
- Assume Processor frequency of 200MHz
- All cache misses result in 32Byte request to SDRAM Buffer
- Assume average subroutine size is 85 Bytes
- Assume code address space spans 512KBytes
- Assume the following code profile (double click on chart to get to the actual numbers on Sheet 1):

Disc Drive Characteristics

- Drive transfers 512Byte Blocks, no interruption is allowed (FIFO overflow == lost data).
- Though transfer rate varies by zone, inter-block time is constant at 800ns.
- 16 Zones each varying in transfer rate
- Assume 13ms “seek” latency when switching between zones.



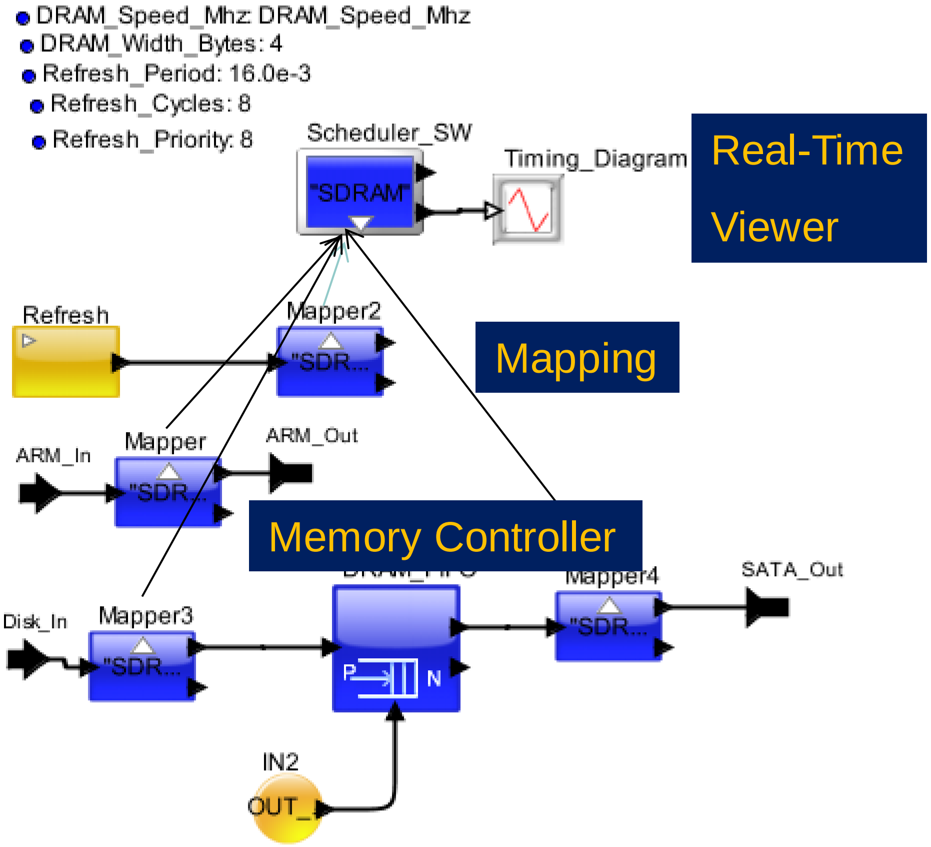
FIFO Characteristics

- Host and Disc FIFOs are distinct, and sized separately
- FIFO width is 32-bits (dWord width)
- FIFO depth can vary between 8 and 128 dWords, in multiples of 8.
- FIFO Almost Full threshold is programmable from 1 to size of the FIFO
- FIFOs do not have any speed dependencies
- SATA FIFO will request transfer from the Buffer when the FIFO is empty, will stop request when FIFO Almost Full
- Disc FIFO will request transfer to the Buffer when the FIFO is Almost Full, and stop request when FIFO empty.

SDRAM Characteristics

- Using single 16-bit DDR SDRAM
- Refresh period set to 16 ms
- CL=3, tRCD=3, tRP=3
- Frequency can be adjusted to 100, 133, or 160 MHz

VisualSim- Component Details- SDRAM



- DRAM_Speed_Mhz: DRAM_Speed_Mhz
- DRAM_Width_Bytes: 4
- Refresh_Period: 16.0e-3
- Refresh_Cycles: 8
- Refresh_Priority: 8

Real-Time Viewer

Mapping

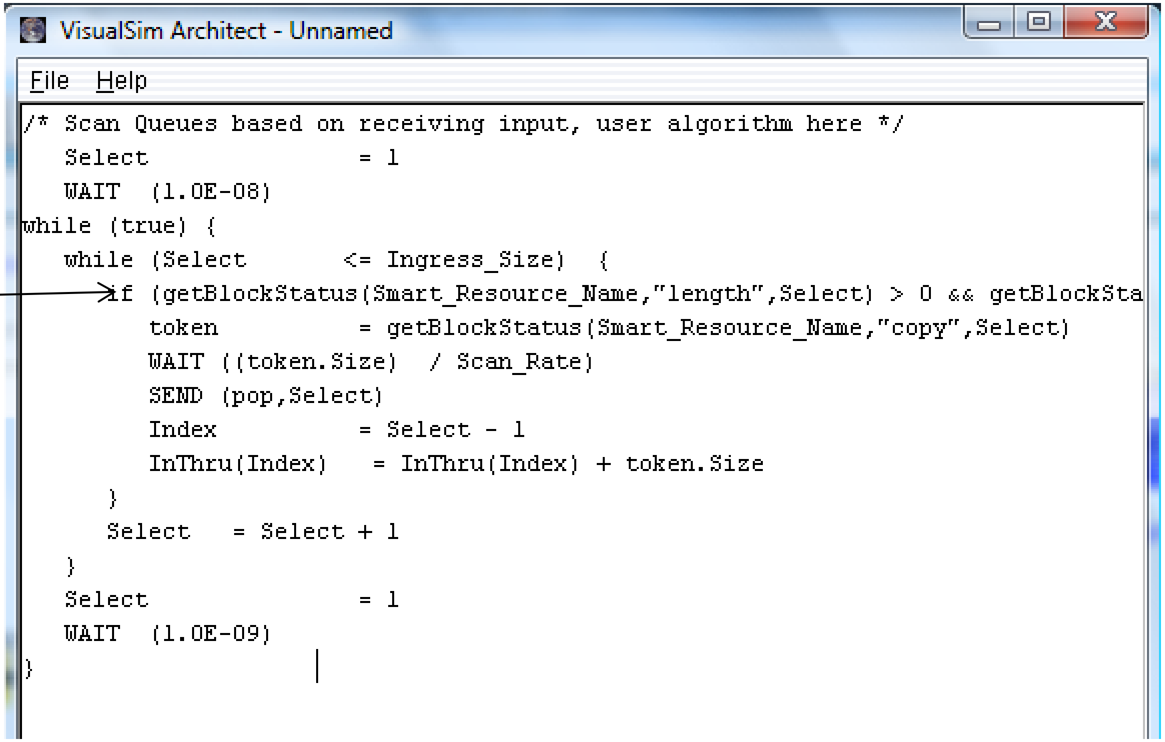
Memory Controller

Client Arbiter Characteristics

- 3 Clients with programmable priority
- Client accesses are 32-bits wide (dWord)
- Client accesses limited to 32Byte bursts
- Assume zero delay for arbitration (pipeline design)

VisualSim- Arbitration

RegEx

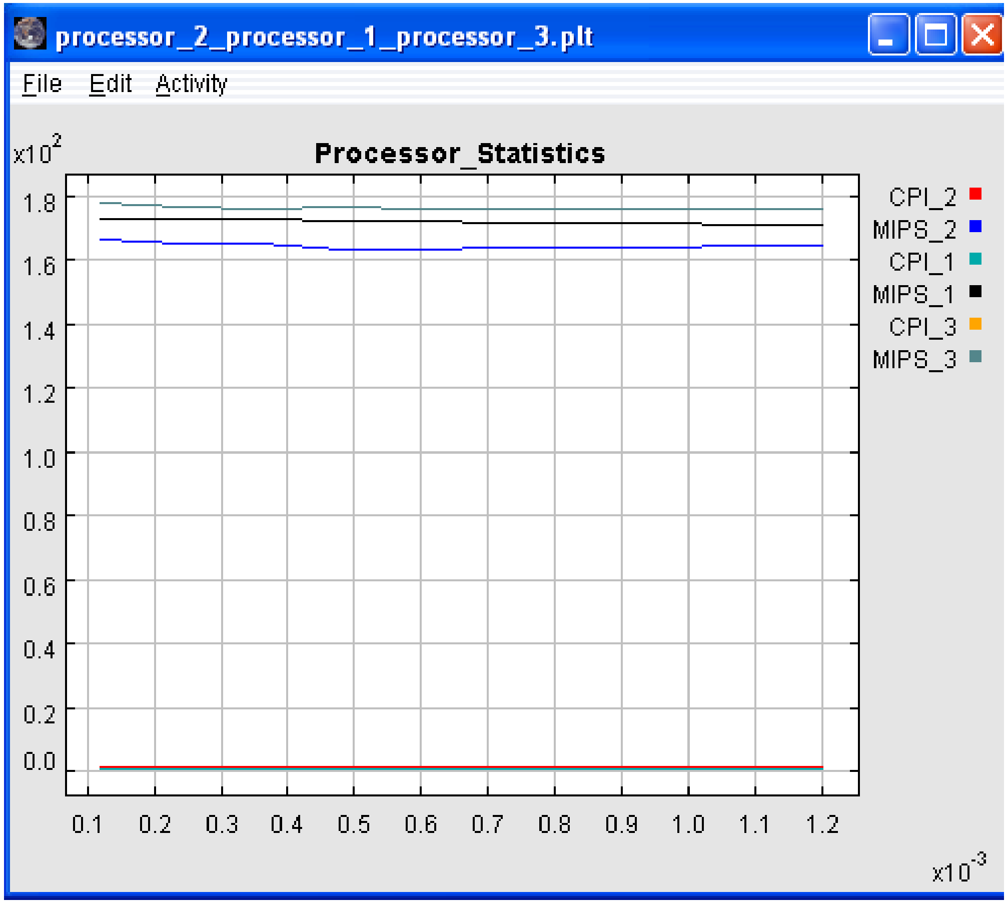


```
/* Scan Queues based on receiving input, user algorithm here */
   Select                    = 1
   WAIT  (1.0E-08)
while (true) {
   while (Select       <= Ingress_Size)  {
      if (getBlockStatus(Smart_Resource_Name,"length",Select) > 0 && getBlockSta
         token           = getBlockStatus(Smart_Resource_Name,"copy",Select)
         WAIT ((token.Size)  / Scan_Rate)
         SEND (pop,Select)
         Index           = Select - 1
         InThru(Index)    = InThru(Index) + token.Size
      }
      Select    = Select + 1
   }
   Select                    = 1
   WAIT  (1.0E-09)
}
```

Simulation Questions & Experiments

- Experiment 1: What SDRAM Frequency do we need?
  - Vary the disc data rate through the zones (ignore seek latencies), but allow each zone to reach steady state
  - Vary SDRAM Frequency between its 3 frequencies
  - Set SATA FIFO to 8 dWords, Disc FIFO to 16 dWords
    - FIFO almost full threshhold set to ¾ FIFO depth
  - Set Arbiter Priority to Disc Highest, Processor Lowest.
  - Monitor average processor instruction latency
  - Monitor SATA throughput & HOLDs
  - Monitor FIFO status

Simulation Results- CPI and MIPS for ARM



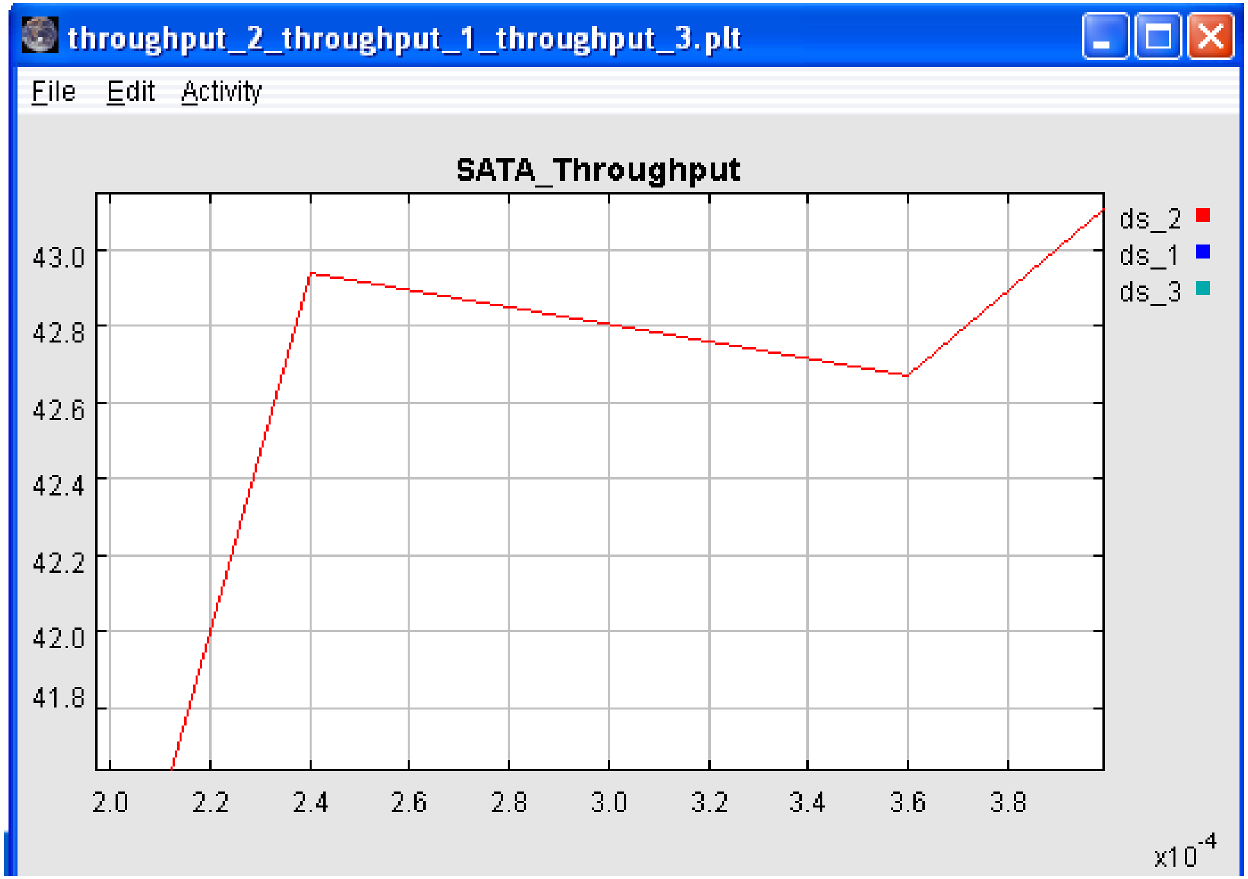
Disk Speed

-100 Mhz

-133 Mhz

-160 Mhz

Simulation Results- Throughput



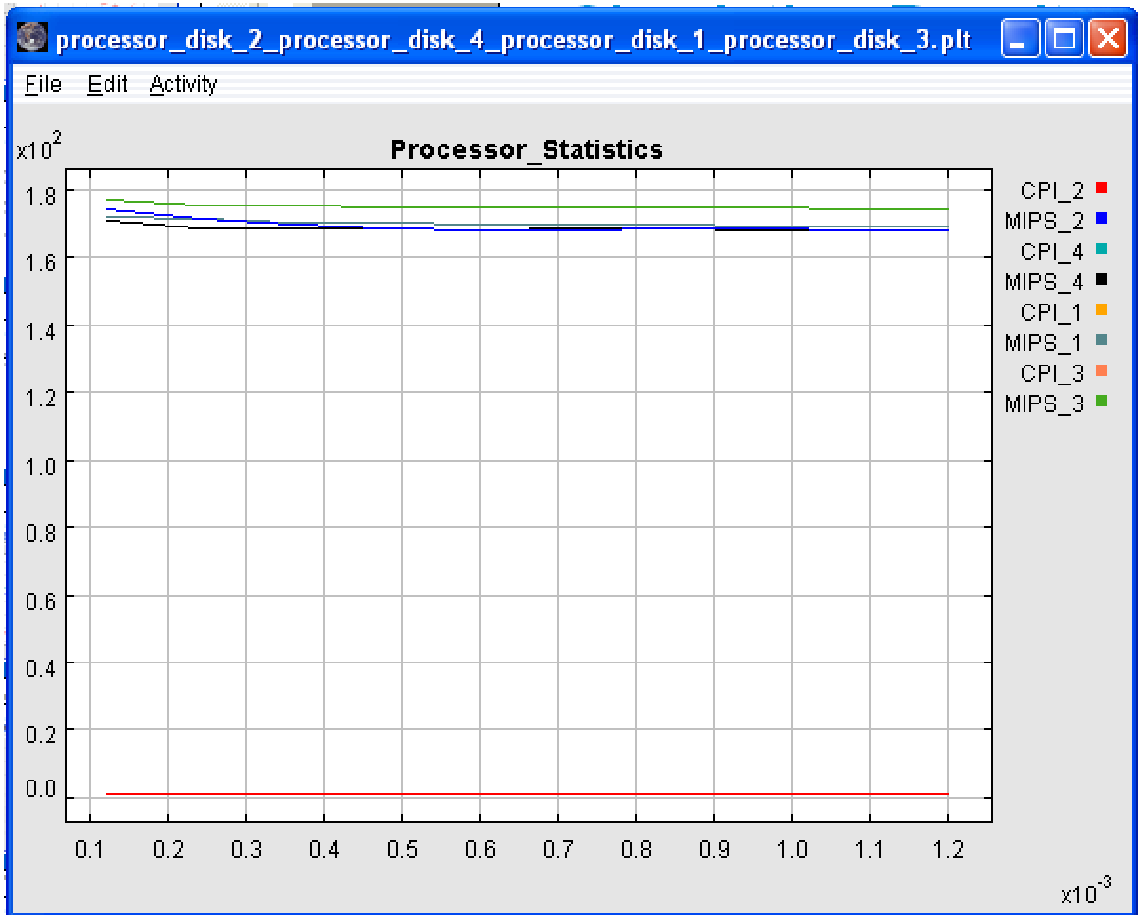
Simulation Result- Analysis

- The DRAM speed (100-160 MHz) did not have a material impact on the Throughput. For this design, the utilization was 41% for 100 MHz and 49% for 160 MHz
- There was a difference in the MIPS at the processor for the different speeds. This was because of the faster response from the DRAM
- -Number of Holds in both cases was 19 during the period of the simulation

Simulation Questions & Experiments

- Experiment 2: Can I lower SDRAM Frequency by adjusting FIFO size?
  - Set the disc data rate to max data rate (zone 1)
  - Set SDRAM Frequency to 133 MHz
  - Set SATA FIFO to 8 dWords
    - FIFO almost full threshhold set to 1/2 FIFO depth
  - Vary Disc FIFO from 8 to 128 dWords incrementing by 8
    - FIFO almost full threshhold set to 3/4 FIFO depth
  - Set Arbiter Priority to Disc Highest, Processor Lowest.
  - Monitor average processor instruction latency
  - Monitor SATA throughput & HOLDs
  - Monitor FIFO status

Simulation Results: Processor Activity



Disk_dWords

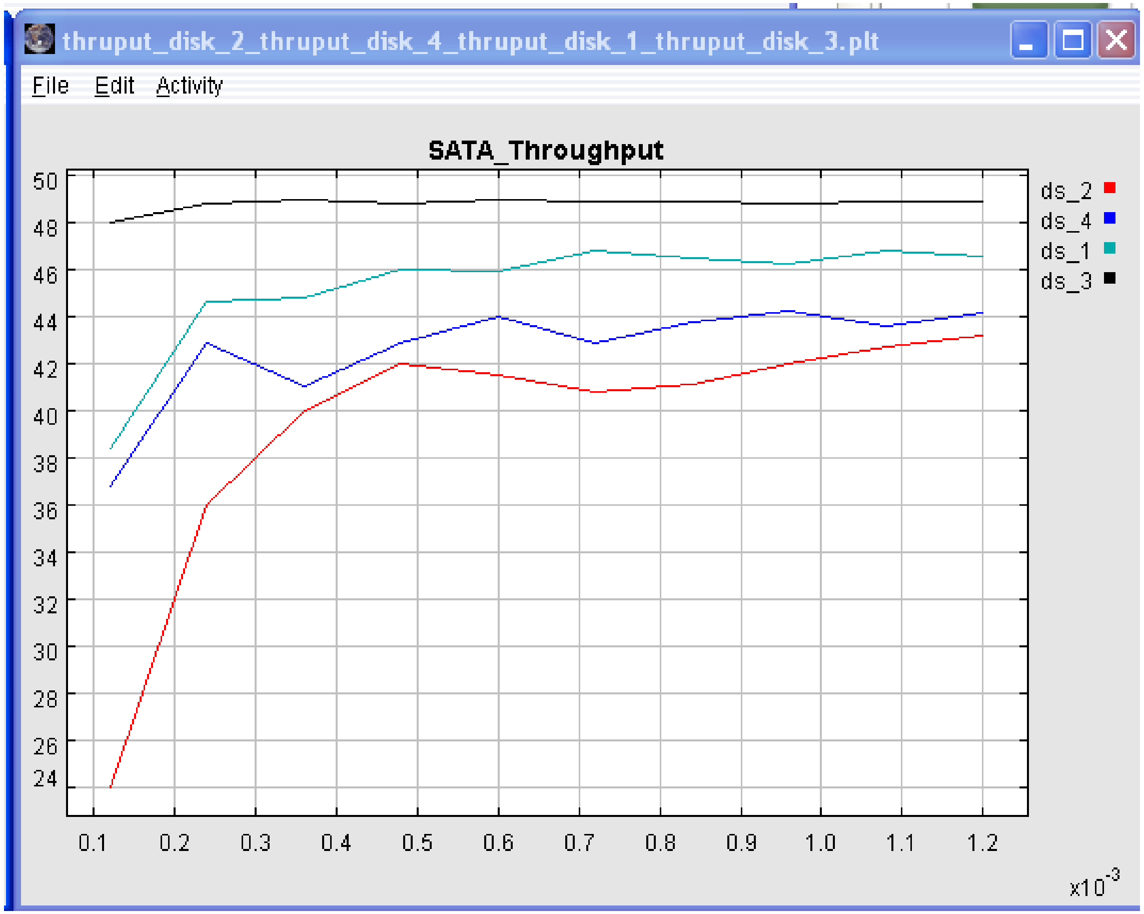
-8

-32

-64

-128

Simulation Results: Throughput



Simulation Questions & Experiments

- What libraries was used to construct the simulation?

Response: Disk model uses Basic Library, Scripting and Controller

A8-R4 Cortex model uses Architecture, Bus-Switch, Power

- What Blocks did you need to modify to construct the simulation?

Response: No modification was required to construct this model

- What Blocks did you need to create to construct the simulation?

Response: Traffic Generator, Randomizer, Database, Probability-based Traffic, Smart Resource, Virtual Machine Script, real-Time plotter and Text display

- Can we vary two variables to get a “surface plot”?

Response: You can vary any number of parameters and combine the results using the Post Processor.

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